

METHOD AND APPARATUS FOR EMULATING A PROCESSOR

Abstract of the Disclosure

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One or more processor operations are emulated in a programmable logic device (PLD) (205) that selectively mimics processor behavior by a program that downloads (505) one or more processor operations into the PLD (205). Each operation may be selected (501) and repeated (513) continuously

10 without interruption from any other processor operation unless such interruption is desired to take place. In addition, the PLD (205) has an adjustable or variable clock speed that provides for the ability to select (507) and change (511) the clock speed under which the test circuit is exercised.

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